# CD Sereis 5

*Firmware Revision History*

*From 7.2.2 to 7.3.3*

*Firmware version 7.3.3 has been released ECO 761*

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### Version 7.2.2                               April 25, 2005.

#### Bug Fixes

The delay that was introduced in order to allow the resolver filter to settle before encoder simulation is enabled was increased to avoid encoder simulation burst after power up

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### Version 7.2.3                               June 20, 2005.

#### Additions and Changes

Support for UVTIME in UVMODE 3.
{UVMODE 3 – drive activate fault only if UV (under voltage) exists and drive is enabled. After UVTIME (under voltage time) elapses, latch fault relay}

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### Version 7.2.4                               June 23, 2005.

#### Bug Fixes

The positive analog power supply to the digital board is monitored during power up. If it is out of tolerances, the firmware locks, and displays flashing A1. Now the firmware limits the time of monitoring the positive analog supply to 6 seconds during power up.

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### Version 7.2.5                               June 29, 2005.

#### Bug Fixes

1. OPMODE 4 (Gearing mode) – getting out of limit switches with wrong feedback position was resolved

2. ZPOS - zpos index parameters were not updated after a change in MSININT (worked ok after power up) was resolved

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### Version 7.2.6                               August 29, 2005.

#### Additions and Changes

Range of MFOLDR (recovery time for motor foldback) was changed from 900 to 3600 to be from 1 to 3600.

#### Bug Fixes

1. SERCOS, in case of MDT error, firmware used corrupted data. In addition: in case of MDT error, firmware extrapolates position and velocity commands.

2. MENCTYPE=10 (for Stegmann) change of PRD direction by MFBDIR did not caused to commutation Initialization, this is caused to incorrect commutation.

3. Initialize serial communication buffers at the end of the initialization process.

4. Software resolver to digital and encoder simulation - the Software resolver to digital tracking filter takes time to stabilize after power up. During this time the encoder simulation module generates false pulses. In order to avoid that, a delay was introduced that waits till the tracking error is stabled (there is a timeout for this delay). During this time the encoder simulation module is off.

## Version 7.2.7                                 September 1, 2005.

### Additions and Changes

1. Added EEPROM command EEMEMW to change/query a specific EEPROM entry, for debug purpose only.

2. Added EEDUMP to get a snapshot of the EEPROM values for debug purpose only.

### Bug Fixes

1. Reset resolver on fault - only on resolver fault (before it was reset on every fault causing false encoder simulation pulses)

2. Move of 1 count in PROFMODE 2.

## Version 7.2.8                                 September 25, 2005.

### Bug Fixes

1. Support for ENDAT with offset on user EEPROM memory added.

2. For sine or resolver feedback "A/B out of range" fault is latched on first occurrence of low range and 3rd occurrence of high range.

## Version 7.2.9                                 October 31, 2005.

### Bug Fixes

Added 2 backgrounds delay after resolver fault reset on drive enable. This delay needed to allow resolver PRD stabilization.

## Version 7.3.0                                 November 22, 2005.

### Additions and Changes

Merged with custom firmware 706a101 to support INITMODE=3 (wake no shake) these are the custom variables XVAR1, XVAR2, XVAR2.

### Bug Fixes

1. Second motion (MI, MA) out of limit switch failed with error message "motion in progress". If you in limit the present point to point move is terminated.

2. Any clear fault in sine encoder caused to reset encoder state machine.

3. In DSP firmware in case of sine encoder and MENCTYPE=0 capture on index was not enabled; there is still problem in ALTERA that sometimes false capture occurs on power up.

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## Version 7.3.1                                          November 27, 2005.

### Bug Fixes

1. False "Index line break" -(r5) fault  indication for sine encoder was fixed.

2. Handle saturation in software resolver to digital at all stages of the SININIT gain and offsets signal corrections.

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## Version 7.3.2                                          January 2, 2006.

### Additions and Changes

INMODE : 32. This input changes the analog command (drive opmode 1,3 and disable) polarity when on. e.g. if analog command  = 5 , in1mode = 32 , ininv1 = 1 :   analog command will be set to -5.

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## Version 7.3.3                                          January 9, 2006.

### Bug Fixes

1. SERCOS phase lock-up at phase 0 was fixed.

2. Error on transition check from SERCOS phase 0 to 2 was canceled. Because of slow background drive sometimes missed phase 1.

3. In baud rates 8,16 SERCON chip synchronization changed to falling edge of RxD signal,  falling edge is more stable and solves missing telegrams problem. (See app note 17-2 for details).

4. Transition of AT telegram at phase 0 was canceled and enabled only at phase 1, this change done to force master(MC) wait for AT telegram and continue send MST with phase 1, otherwise master almost immediately sends phase 2.